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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,127	11/25/2003	Yu-Chuan Lin	LINY3047/EM	4399

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EXAMINER	
PATEL, KAUSHIKKUMAR M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,127	LIN ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claims 7, 19-20 are objected to because of the following informalities:

Claim 7 depends from claim 5. It is understood that claim 7 should depend from claim 6, and treated as such for the remainder of this office action.

Applicant is advised that should claim 19 be found allowable, claim 20 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before

the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (US 2004/0080998 A1) (Chang herein after).

As per claim 1, Chang teaches a device for recording block status information of a nonvolatile memory (see abstract and fig. 1), comprising:

an interface unit (fig. 2a, item 130) electrically connected to at least one nonvolatile memory (fig. 2a, item 124) including a plurality of blocks (fig. 2b, item 11), each being a basic unit for erasing data of said at least one nonvolatile memory (page 3, paragraph [0036]);

a processor connected to said interface unit through which the status of a block of said at least one nonvolatile memory is detected to obtain the block status information (fig. 2a, item 108, page 3, paragraph [0037]); and

a memory unit connected to said processor for temporarily storing said block status information which is then written into one of said plurality of blocks by means of said processor through said interface unit after end of the detection (fig. 2b, item 21, paragraph [0048], taught as data to be programmed into to blocks or data read from blocks and status of data are typically stored in a buffer memory within control system temporarily).

As per claim 2, Chang teaches a device for recording the block status information, comprising a counter for counting the number of the blocks of said at least one nonvolatile memory when said processor detects the status of the blocks of said at least one nonvolatile memory to obtain a counter value so that

said processor writes said counter value into said at least one nonvolatile memory after the end of the detection (page 5, paragraphs [0052], [0061] and [0065], taught as processor executes software or firmware to control nonvolatile memory and erase count block keeps track of usable and unusable blocks).

As per claims 3, 4 and 5 Chang teaches device which contains erase count block and keeps track of the valid or invalid blocks (paragraphs [0065] and [0067]). Thus Chang implicitly teaches counter value is the number of valid or invalid blocks and also valid and invalid block addresses.

As per claims 6 and 7, Chang teaches that a nonvolatile memory device is a removable nonvolatile memory and arranged to interface with bus to store information (paragraph [0043]). Thus Chang inherently teaches that interface unit is host device and removable memories are known to be house in an integrated circuit sockets.

As per claim 8, Chang teaches that one of plurality of blocks is the first block (block 0) (fig. 2b, item 11).

As per claim 9, Chang teaches that signatures are used to identify the faulty blocks (fig. 2b. item 23, paragraph [0063])

As per claim 10, Chang teaches memory unit is random access memory (RAM) (fig. 2a, item 112)

As per claim 11, Chang teaches nonvolatile memory is a NAND-type flash memory (paragraph [0044]).

As per claim 12, Chang teaches a method for performing the block status information (fig. 1) of nonvolatile memory, comprising:

(a) performing an initialization to set reference value (paragraph [0066], taught as erase count block is initialized);

(b) detecting nonvolatile memory having a plurality of blocks to obtain the status of at least one block which is a basic unit for erasing data of the at least one nonvolatile memory (paragraph [0049]);

(c) writing the detected information into a memory unit until the end of the detection, and then writing said at least one block status information into one of the blocks of said at least one nonvolatile memory. (taught as information from nonvolatile memory is stored temporarily stored in the buffer memory (paragraph [0048]) and information regarding valid and invalid blocks is stored in the erase count block as taught in claims 1-6 above).

Claims 13-21 are rejected under the same rationale as applied to claims 2-11 above.

Conclusion

The prior art made of record and not relied upon is pertinent to applicant's disclosure. Chow et al. (US 2003/022591 A1) teaches method and apparatus for maintaining and detecting free blocks as well as bad blocks of a nonvolatile memory and flash status information.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

12/5/05